06-04-03

AFA

Attorney's Docket No. 64,600-065

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Shyh-Ming Chang
Serial No.: 09/ 634,556
Filed: August 7, 2000
For: Method for Forming Electrically Conductive Bumps and Devices Formed

Group Art Unit: 2813
Examiner: Thanhha S. Pham

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on March 31, 2003.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT

This application is on behalf of:

X other than a small entity.
___ a small entity.

A verified statement:

___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

___	small entity	$160.00
X	other than a small entity	$320.00

Appeal Brief fee due: $ 320.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

Mailing

X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EV 261 230 833 US in an envelope addressed to Box Appeal, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Kathy Dixon

Dated: June 2, 2003

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 390.00	$195.00
☐	three months	$ 930.00	$465.00
☐	four months	$1,470.00	$735.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 320.00
Extension fee (if any) $_____

TOTAL FEE DUE: $ 320.00

6. FEE PAYMENT

X Attached is a Credit Card Payment Form for the sum of $ 320.00
X Charge American Express Credit Card No. 3715 663193 71002 the sum of $ 320.00.
A duplicate copy of this transmittal is attached.

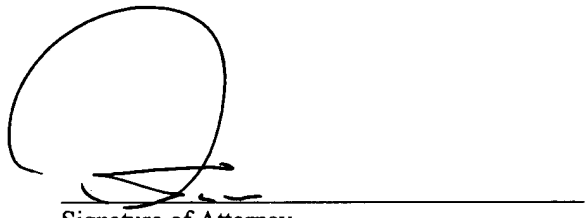
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

__X__ If any additional extension and/or fee is required, this is a request therefor to charge American Express Credit Card No. 3715 663193 71002

And/Or

__X__ If any additional fee for claims is required, please charge American Express Credit Card No. 3715 663193 71002



Signature of Attorney

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant: Shyh-Ming Chang

Group Art Unit: 2813

Serial No.: 09/634,556

Examiner: Thanhha S. Pham

Filed: Aug. 7, 2000

For: Method for Forming Electrically Conductive Bumps and Devices Formed

Attorney Docket No.: 64,600-065

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EV 261 230 833 US
Date of Deposit June 2, 2003

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $320.00 (required filing fee) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Box Appeal, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Kathy Dixon

APPEAL BRIEF

Box Appeal
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants appeal in the captioned application from the Examiner's final rejection, dated December 31, 2002, of claims 1-16, under 35 USC §103(a) as being unpatentable over Appellants' admitted prior art, Chang et al '697, Estes et al '208 and Farnworth et al '930.

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It is urged that the rejection be reversed and that all the claims be allowed.

(1) REAL PARTY IN INTEREST

The real party in interest in the present appeal is the recorded Assignee of Industrial Technology Research Institute.

(2) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that are known to the Appellants, the Appellants' legal representative, or the assignee.

(3) STATUS OF CLAIMS

Claims 1-16 are pending in the application.

Claims 1-16 stand rejected.

(4) STATUS OF AMENDMENTS

A Request For Reconsideration was filed on or about February 28, 2003, which contains no claim amendments.

An Advisory Action was received from the Examiner dated March 11, 2003 rejecting all claims.

A Notice of Appeal was filed on or about March 31, 2003.

(5) SUMMARY OF THE INVENTION

The invention relates to a single-stencil and single-mask process for forming electrically conductive, compliant bumps on a wafer and devices formed by the method.

(Specification, page 1, lines 6-8)

In a preferred embodiment, a method for forming electrically conductive bumps on a wafer can be carried out by the operating steps of first providing a wafer that has an active surface, a plurality of conductive elements formed on the active surface, and a passivation layer insulating the plurality of conductive elements from each other; sputter depositing a first metal layer on top of the plurality of conductive elements and the passivation layer; printing a plurality of bumps of an insulating material each on top of one of the plurality of conductive elements; heat treating the plurality of bumps at a temperature of at least 100°C; sputter depositing a second metal layer on top of the plurality of bumps and the first metal layer; and patterning and removing the first and the second metal layer in areas in-between the plurality of bumps.

(Specification, page 11, lines 1-14)

(6) **ISSUE**

Issue I

Is the rejection of claims 1-6 and 14-16 under 35 USC §103(a)as being unpatentable over appellants' admitted prior art in view of Chang et al '697, proper when such references do not teach or suggest the specifically claimed limitations in the present application?

Issue II

Is the rejection of claims 7-13 under 35 USC §103(a) as being unpatentable over appellants' admitted prior art in view of Chang et al, Estes et al '208 and Farnworth et al '930, proper when such references do not teach or suggest the specifically claimed limitations in the present application?

(7) **GROUPING OF CLAIMS**

The rejection of claims 1-6 and 14-16 are contested as a group.

The rejection of claims 7-13 is contested as a separate group.

(8) **ARGUMENTS**

Issue I

Claims 1-6 and 14-16 are rejected under 35 USC §103(a) as being unpatentable over appellants' admitted prior art in view of Chang et al '697. It is contended that the appellants' prior art disclosure substantially discloses the claimed method for performing electrically conductive bumps on a wafer including the steps of **printing a plurality of bumps** of an insulating material each on top of one of said plurality of conductive elements. It is further contended that the appellants' prior art disclosure only failed to teach heating the plurality of bumps at a temperature of at least 100°C, which is disclosed by Chang et al.

The rejection of claims 1-6 and 14-16 under 35 USC §103(a) based on appellants' prior art disclosure and Chang et al is improper and must be reversed.

The appellants respectfully submit that, contrary to the Examiner's contention, the appellants' own prior art disclosure does not disclose a method in which a plurality of bumps are printed. To the contrary, as disclosed in the specification at line 11, page 6 through line 9, page 7:

> "An insulating material layer 20, possibly of a polymeric-based material, is then **coated** on the semiconductor substrate 10 encapsulating the first metal layer 18. The insulating material layer 20 can be advantageously applied ... by a method such as **spin coating**. ...
> After a photolithographic process is conducted on the polymeric material layer 20, the layer is dry or wet etched forming a plurality of electrically insulating bumps 22 on top of the first metal layer 18. ..."

Similarly, Chang et al '697 does not teach a method of printing a plurality of bumps. For instance, as recited in claim 1 of Chang et al:

> "... forming a polymer layer on the surface of said integrated circuit element or substrate;
> forming a first photoresist mask on said polymer layer directly over said input/output pads;
> etching said polymer not protected by said first photoresist mask;
> ..."

Contrary to the appellants' own prior art disclosure and Chang et al, the present invention, as clearly recited in independent claim 1, teaches a process in which:

> "Claim 1. A method for forming electrically conductive bumps on a wafer comprising the steps of:
>
> providing a wafer ...,
>
> sputter depositing a first metal layer ...,
>
> **printing a plurality of bumps** of an insulating material each on top of one of said plurality of conductive elements,
>
> ...,
>
> ..., and
>
> ..."

In the Response To Argument section of the 12/31/2002 Office Action, the Examiner argues that "contradictory to appellants' argument on pages 2-4 that the appellants' own prior art disclosure does not disclose a method in which a plurality of bumps are printed, appellants' admitted prior art discloses the method in which the plurality of bumps are **printed by a photolithographic process**" and furthermore, "those skilled in the art must recognize that the bumps 22 of APA are formed by using

photoresist masks wherein **shapes of the bumps 22 are printed from the shapes of photoresist masks**. The plurality of bumps 22 are, therefore, printed each on top of one of the plurality of conductive element 14". The Examiner then cited a definition for "print" from Merriam Webster's Collegiate Dictionary "produce printed matter" or "display on a surface for viewing".

The appellants respectfully submit that the Examiner's argument is flawed since the phase "printing a plurality of bumps" recited in the claims is to be interpreted by one skilled in the art, and not by a definition from the Webster's Dictionary. **To one skilled in the art in the fabrication technology of semiconductors, the word "printing" used in the context of "printing a plurality of bumps" would mean stencil printing or screen printing**, and not printing an image on a surface for viewing as cited by the Examiner from Webster's Dictionary. To one skilled in the art in the semiconductor processing technology, printing would mean stencil printing or screen printing by using a stencil, a screen in the shape of a template. **A photolithographic process would have nothing to do with the technology of stencil printing or screen printing**. As a matter of fact, **the appellants have exhaustively explained the difference between the present invention printing technology vs that of a photolithographic thin film process** in the

specification at page 19, line 1 through page 20, line 15. Specifically, at line 7 of page 19:

> "The disadvantage of the printing method is that the pitch distance between the bumps 60 is limited to a minimum of about 100 μm. This is compared to a smaller pitch distance of about 10 μm achievable by the thin film method of photolithography."

Issue II

Claims 7-13 are rejected under 35 USC §103(a) as being unpatentable over appellants' admitted prior art in view of Chang et al, and further in view of Estes et al '208 or Farnworth et al '930. It is contended that the appellants' prior art disclosure in view of Chang et al substantially discloses the claimed method except teaching using stencil printing to print the plurality of bumps.

The rejection of claims 7-13 under 35 USC §103(a) based on appellants' admitted prior art, Chang et al, Estes et al and Farnworth et al is improper and must be reversed.

While the appellants agree with the Examiner that the appellants' admitted prior art in view of Chang et al does not teach using stencil printing to print the plurality of bumps, the appellants submit that the unique printing step and sputter coating step followed thereafter are not taught or disclosed by Estes et al or Farnworth et al.

The appellants respectfully submit that the plurality of bumps printed by the present invention method is distinctly different than that printed by the Estes et al or Farnworth et al methods. The bumps printed by the present invention are formed of an insulating material, **a secondary process of sputter depositing a layer of metal on top of the insulating bumps is required to make the bumps electrically conductive.** This is clearly stated in independent claim 1:

"...,

...,

printing a plurality of bumps of an insulating material ...,

...,

sputter depositing a second metal layer on top of said plurality of bumps and said first metal layer, and

..."

The two-step forming process of the present invention bumps is patentably distinct from that of the one-step bump forming process of Estes et al and Farnworth et al in which **electrically conductive** polymer bumps are stencil printed on flip-chips.

Moreover, the appellants respectfully submit that since the Estes et al or Farnworth et al's printing of electrically conductive polymer bumps is conducted on flip-chips, while the present invention printing method of insulating polymeric bumps is conducted on a wafer (wafer level packaging process). The two techniques are patentably distinct.

The rejection of claims 7-13 under 35 USC §103(a) based on the appellants' admitted prior art, Chang et al, Estes et al and Farnworth et al is improper and must be reversed.

CLOSING

In summary, the Appellants have shown that their claimed invention is fully supported by a body of evidence of non-obviousness. It is therefore respectfully submitted that such evidence of non-obviousness overcomes any showing of obviousness

presented by the Examiner. The Appellants therefore submit that the final rejection of their claims 1-16 is improper under 35 USC §103(a).

The reversal of the final rejection is respectfully solicited from the Board.

Respectfully submitted,

Tung & Associates

By: _____

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CLAIM APPENDIX

1. A method for forming electrically conductive bumps on a wafer comprising the steps of:

providing a wafer having an active surface, a plurality of conductive elements formed on the active surface, and a passivation layer insulating said plurality of conductive elements from each other,

sputter depositing a first metal layer on top of said plurality of conductive elements and said passivation layer,

printing a plurality of bumps of an insulating material each on top of one of said plurality of conductive elements,

heat treating said plurality of bumps at a temperature of at least 100°C,

sputter depositing a second metal layer on top of said plurality of bumps and said first metal layer, and

patterning and removing said first and said second metal layer in areas in-between said plurality of bumps.

2. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of forming said plurality of conductive elements spaced-apart by at least 100 μm.

3. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of forming said plurality of conductive elements in aluminum or copper.

4. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of forming said passivation layer in an insulating material.

5. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of sputter depositing said first metal layer in a material selected from the group consisting of Al, Ni, Ti, W, Cu, Cr and alloys thereof.

6. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of sputter depositing said first metal layer to a thickness not higher than 50 μm.

7. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique.

8. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique in a polymeric material.

9. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique in polyimide.

10. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique to a width of at least 50 μm.

11. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique to a thickness of at least 20 μm.

12. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique in a polymeric-based paste.

13. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of printing said plurality of bumps by a stencil printing technique in a solvent-containing polymeric paste.

14. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of depositing said second metal layer in a material selected from the group consisting of Al, Ni, Ti, W, Pt, Pd, Cu, Cr, Ag, Au, In, Sn, Pb and alloys thereof.

15. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of patterning said first and said second metal layer by a photolithographic method.

16. A method for forming electrically conductive bumps on a wafer according to claim 1 further comprising the step of removing said first and said second metal layers by a photolithographic and a wet etch method.